LONG DELAY TRANSISTOR TIMER *

by P. Aderisio

I. INTRODUCTION

A convenient method of time delay is to use an RC network where the voltage developed across the capacitor operates a relay, preferably through a bistable circuit. The accuracy of this method depends on the exponential characteristic of the RC network. Long time delays require large time constants so that the triggering level is set without appreciable departure from a linear characteristic. Furthermore, when the RC network is followed by a low impedance transistor circuit, the shunting effect on the capacitor must be minimized which often requires very large capacitance values.

In order to reduce the time constant needed for a given delay, a Miller integrator circuit, as analyzed in the Appendix, may be used to advantage. With this circuit it is possible to use time constants even smaller than the time delay required, with the additional advantage of stable operation irrespective of transistor gain.

II. DESCRIPTION OF THE CIRCUIT

With reference to Fig. 1, transistors T_1 and T_2 form a Miller integrator circuit with a switchable resistor R at the base of T_1 and a feedback capacitor C from the collector of T_2 to the base of T_1. The timing circuit is followed by a bistable circuit formed by T_3 and T_4. Transistor T_3 operates the relay R_L. Switch S_1 may be replaced by a diode D_1 if preferred.

In the rest condition, S_1 and S_2 are closed (D_1 is conducting, if present); C is charged at V_1 volts, and as V_1 is less than V_2, T_2 is conducting and T_1 is cut-off. Also, D_2, T_4, and T_3 are non-conducting, and the relay is not energized. Operation starts by opening S_1 and S_2 which causes the collector voltage of T_2 to jump in the positive direction.

As the charge of the capacitor, C, cannot change abruptly, the jump is transferred to the base of T_1, cutting off D_1 if present, and causing conduction of T_1. Conduction of T_1 tends to cut-off T_2, with the result that the voltage step at the collector of T_2 is limited to $(V_2 - V_1)$ volts approximately, neglecting the difference of the voltage drops across the emitter-to-base junctions of T_1 and T_2. After the initial step, the collector voltage of T_2 rises linearly with time (see Appendix 1). As the voltage at the junction of R_5 and R_6 reaches V_3 volts, D_2 and T_4 start conducting and the collector current of T_4 drives T_3 into conduction causing the collector voltage of T_3 to rise. Regenerative action occurs at this point through positive feedback to the base of T_4 and the relay is energized.

As the collector of T_2 is a low impedance point, resistor R_5 has the function of establishing a sufficient degree of positive feedback for the bistable circuit. Capacitor C_1 prevents the bistable circuit from being triggered by spurious pulses. The circuit is reset by closing S_2 and S_1, if present.

T_1 and T_2 form a compound Darlington amplifier. Over the conventional Darlington connection this has the advantage that the resultant V_{BE} has a low thermal coefficient, the total V_{BE} being the difference of the V_{BE}'s of the NPN and PNP transistors. The minimum current gain G of the amplifier may be taken as one thousand times. With the values relative to Fig. 1, equation (12A) holds with good approximation, apart from the sign which is positive in this case. The positive sign arises from the initial condition with C charged at the potential V_1. Taking also in account the initial voltage jump we have, at the junction of R_5 and R_6:

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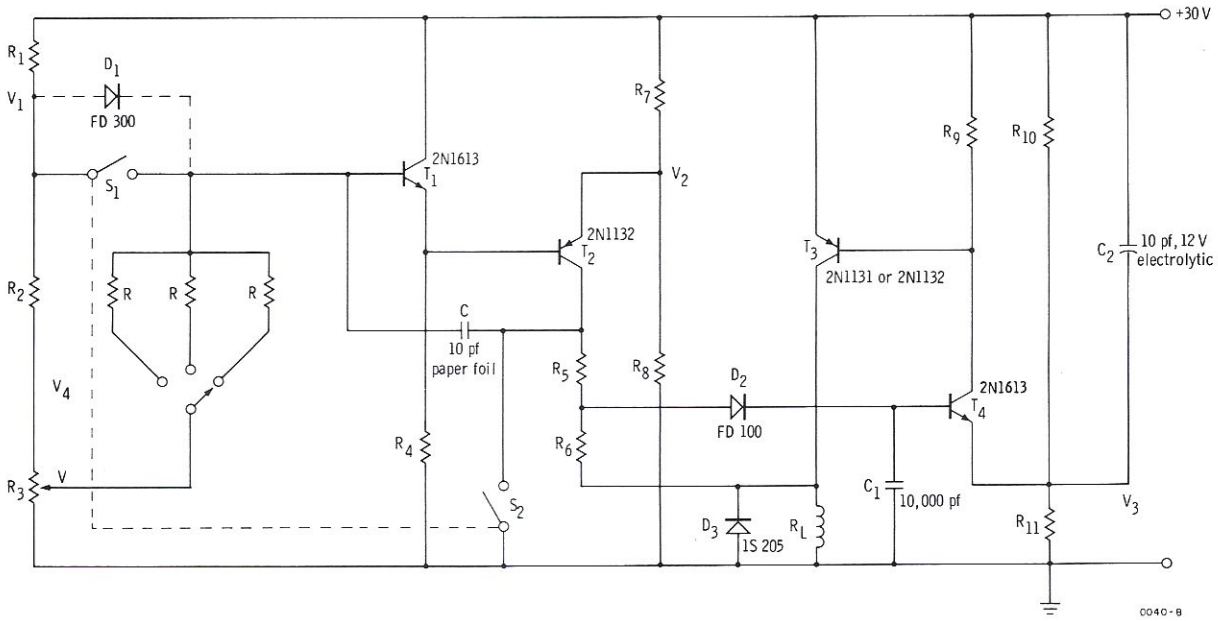

R_1	-	1 K Ohm	1%	R_5	-	10 K Ohm	5%	R_9	-	1 K Ohm	5%	R	100 K Ohm	1%
R_2	-	1.5 K Ohm	1%	R_6	-	100 K Ohm	5%	R_{10}	-	2 K Ohm	1%	R	0.5 K Ohm	1%
R_3	-	10 K Ohm	wire wound	R_7	-	100 K Ohm	1%	R_{11}	-	10 K Ohm	1%	R	2 M Ohm	1%
R_4	-	3.3 M Ohm	5%	R_8	-	2.7 K Ohm	1%	R_L	-	5 K Ohm	Relay			

FIG. 1. Schematic for electronic timer with delays from 1 to 100 seconds.

$$V_0 = \left(V_2 - V_1 + \frac{V_2 - V}{CR}\, t\right) \frac{R_6 + R_L}{R_5 + R_6 + R_L} \qquad (1)$$

for $V_0 = V_3$, $t = T$, and with the values of Fig. 1:

$$V_2 = 29 \text{ volts}$$
$$V_1 = 27.6 \text{ volts}$$
$$V_3 = 25 \text{ volts}$$

Therefore

$$T \approx \frac{26\ CR}{29\ V} \qquad (2)$$

For a given R, maximum delay is achieved when $V = V_4 = 24$ volts, minimum delay when $V = 0$. Maximum and minimum delays have been calculated with the aid of equation (2) for the three resistance values shown in Fig. 1, and the results compared with measurements in Table 1.

TABLE 1

R	T_{max} seconds		T_{min} seconds	
Mohms	Calculated	Measured	Calculated	Measured
0.1	5.2	5.2	0.9	
0.5	26.0	25.8	4.5	4.6
2	104.0	100.2	18.0	17.8

It was not possible to measure accurately the time in the last column, first row. The measurements were taken at 22°C and the results shown in Table 1 are the average of several measurements. At 50°C negligible variations were measured. Under extreme conditions and for a temperature range from 0°C to +50°C, the measurements checked with better than two percent accuracy.

Equation (2) suggests that the delay time control can be made linear if R is varied and V is fixed.

The general expression, derived from Eq. (1)

$$T = \frac{R_5 + R_6 + R_L}{R_6 + R_L} \frac{V_3\ CR}{V_2 - V_1} - \frac{V_2 - V_1}{V_2 - V} CR \qquad (3)$$

shows that the time delay T is independent of supply voltage variations provided that all the reference potentials are made proportional to the supply voltage. In order to check this point, new measurements were taken at supply voltages lower than nominal. Negligible errors were measured down to -10% of the supply voltage.

APPENDIX

I. ANALYSIS OF A MILLER INTEGRATOR EMPLOYING A CURRENT AMPLIFIER

With reference to Fig. 1A, it is assumed that the amplifier has a current gain, G, and an input resistance, R_i. A condenser, C, is connected between the input and the output of the amplifier and a d-c voltage, V, is suddenly applied at the input through a resistance, R.

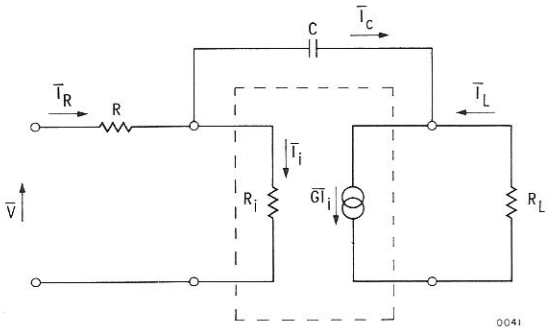

FIG. 1A. Equivalent circuit of Miller integrator.

The following equations may be written:

$$\begin{cases} (R + R_i)\,\bar{I}_i + R\,\bar{I}_c = \bar{V} \\ G\bar{I}_i - \bar{I}_i - \bar{I}_c = 0 \\ R_i\bar{I}_i + R_L\bar{I}_L - \dfrac{\bar{I}_c}{pC} = 0 \end{cases} \tag{1A}$$

where $\bar{I}_i$, $\bar{I}_L$, $\bar{I}_c$ are functions of the complex variable p.

Solving for $\bar{I}_L$

$$\bar{I}_L = \bar{V}\,\frac{G + pCR_i}{R + R_i + pC\left[RR_L(1 + G) + R_i(R + R_L)\right]} \tag{2A}$$

Setting

$$R^* = \frac{RR_L(1 + G) + R_i(R + R_L)}{R + R_i} \tag{3A}$$

Results in

$$\bar{I}_L = \bar{V}\,\frac{G + pCR_i}{(R + R_i)(1 + pCR^*)} \tag{4A}$$

Assuming that $\bar{V}$ is a step function, $\bar{V} = V/P$, therefore

$$\bar{I}_L = \left(\frac{VG}{R + R_i}\right)\left(\frac{1}{p(1 + pCR^*)}\right) + \frac{VCR_i}{1 + pCR^*} \tag{5A}$$

which may also be written:

$$\bar{I}_L = \frac{VG}{R + R_i}\left(\frac{1}{p} - \frac{1}{p + \frac{1}{CR^*}}\right) + \frac{VR_i}{(R + R_i)R^*}\,\frac{1}{p + \frac{1}{CR^*}} \tag{6A}$$

Applying the inverse Laplace transform, I_L, as a function of time is given by:

$$I_L = \frac{VG}{R + R_i}\left[1 - \exp(-t/CR^*)\right] + \frac{VR_i}{(R + R_i)R} \times \exp(-t/CR^*) \tag{7A}$$

If $CR \gg t$, series expansion of the exponential term yields:

$$I_L \approx \left(\frac{VG}{R + R_i}\right)\left(\frac{t}{CR}\right) + \left(\frac{VR_i}{(R + R_i)R^*}\right)\left(\frac{t}{CR^*}\right) \tag{8A}$$

$$I_L \approx \frac{Vt}{(R + R_i)CR^*}\left(G + \frac{R_i}{R^*}\right) \tag{9A}$$

which is a linear function of time.

With a transistor amplifier with large value of G, R^* can be made much larger than R_i, therefore:

$$I_L \approx \frac{VGt}{C\left[RR_L(1 + G) + R_i(R + R_L)\right]} \tag{10A}$$

If the gain, G, is large and R_i small, the second term at the denominator can be neglected. Therefore the output voltage is simply given by

$$V_0 = \left(-\frac{G}{G + 1}\right)\left(\frac{Vt}{CR}\right) \tag{11A}$$

As $G \gg 1$ $$V_0 = -\frac{V}{CR}t \qquad (12A)$$

which is independent of G.

II. COMPARISON BETWEEN CONVENTIONAL RC TIMERS AND THE MILLER INTEGRATOR

Three cases will be considered:

a. Simple RC network

b. RC network followed by an amplifier

c. Miller circuit.

For all the cases it will be assumed that the triggering level, V_t, is affected by a drift ΔV_t. In order to minimize the timing error due to the drift, it is necessary that the triggering level be as large as possible compared to ΔV_t. Furthermore, the triggering level must be set at a point where no appreciable departure from the linear characteristic exists.

Case a requires that the aiming voltage, V_a, of the network be much larger than V_t and that the RC product be much larger than the time delay, T, required. The network must be followed by a high input impedance circuit.

For the case b the aiming V_b can be the same as or less than V_t, but the RC product must be as in case a. The amplifier must have a high input impedance and have a voltage gain V_a/V_b for the same performance of case a. The gain of the amplifier must be stable.

For case c the aiming voltage can be as in case b, the RC product can be less than the time delay T, the condition to be satisfied being $(G + 1) R_L C \gg T$, and the amplifier input impedance should preferably be low. The last condition is easily met with transistor amplifiers. If G is sufficiently large, the output voltage is not affected by variation of gain.

The case $R_i = 0$ is particularly simple and the equation (7A) yields:

$$V_0 = -\frac{VGR_L}{R}\left\{1 - \exp\left[-t/(G + 1)R_L C\right]\right\} \qquad (13A)$$

or

$$V_0 = -\frac{VGR_L}{R}\left[1 - \exp\frac{-t}{(G + 1) RCR_L/R}\right] \qquad (14A)$$

which suggests that the equivalent circuit of Fig. 1A is a series resistance-capacitance network composed of R and of a capacitance $C(G + 1) R_L/R$. The aiming potential of the network is V.

The network is followed by an infinite input resistance amplifier having a transconductance, G/R, loaded by a resistance, R_L; see Fig. 2A.

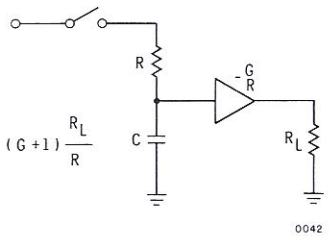

FIG. 2A. Miller network followed by infinite input resistance amplifier.

It is important to note that if G is sufficiently large, the performance is not affected by variation of G.

REFERENCE

E. Wolfendale, The Junction Transistor and Its Applications, p. 308, 1958.

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